

INSULATED GATE SEMICONDUCTOR DEVICE WITH EXTRA SHORT GRID AND METHOD OF FABRICATION

BACKGROUND OF THE INVENTION

The present invention relates to insulated gate semiconductor devices and more particularly to those insulated gate devices which are susceptible to achieving a non-preferred latched state of operation. Insulated gate devices which are susceptible to latching include insulated gate transistors, insulated gate thyristors, and other MOS controlled devices which have one or more inherent bipolar transistors included therein. Under latched operating circumstances, the base emitter junction of the inherent transistor can become forward biased causing the device to continue to conduct current even though the gate drive has been turned off. Thus, insulated gate control of the device can be lost and it is then generally necessary to remove the forward bias potential and/or commutate the device to stop current flow and to turn the device off.

Referring now to FIG. 1, a conventional insulated gate transistor comprising four layers of alternate conductivity material is shown. A cathode electrode is disposed in ohmic contact with the base and source regions. An insulated gate is disposed over the base and conductively couples opposite type conductivity carriers from the cathode through a base region gate induced channel into the drift region of the device. At the same time, one type conductivity carriers flow through the base and drift regions between the anode and the cathode electrode. One type conductivity carriers, however, flowing along the PN junction between the base and emitter regions can establish a voltage drop V along this junction. In the event the voltage drop along this junction exceeds approximately 0.7 volts in a silicon device, the junction can become forward biased causing the upper NPN transistor to conduct. Once activated, the upper transistor establishes a regenerative conduction relationship with the lower PNP transistor so that the device as a whole functions as a silicon controlled rectifier or thyristor which is regeneratively latched into a conductive state. Insulative gate control of this device is thus lost.

OBJECTS OF THE INVENTION

A principal object of the present invention is therefore to provide improved insulated gate semiconductor devices in which the inherent transistors are less susceptible to being inadvertently activated or turned on to render uncontrolled or latched conduction less possible.

It is further object of the present invention to provide an improved insulated gate semiconductor device in which a high conductivity alternate current path is established proximate the PN junction to thus reduce the current flow within the region adjacent the PN junction and hence voltage drop adjacent the PN junction.

Another object of the present invention is to provide a high voltage insulated gate semiconductor device which efficiently employs a one type conductivity grid structure proximate a one type conductivity base region to facilitate conduction of one type carriers outside the base region of the device without imposing an unnecessary voltage drop on the base emitter PN junction.

A still further object of the present invention is to provide an insulated gate semiconductor device em-

ploying a grid structure comprising a plurality of separate regions disposed within the drift region of the device to provide for direct contact between the drift and base regions of the device and to provide an alternate current path for minority carrier flow within the device.

An additional object of the present invention is to control the doping concentration and depth of the various regions of the device to minimize the on-resistance within the minority carrier current path to minimize the voltage drop in that path.

SUMMARY OF THE INVENTION

These and other objects and features of the present invention are achieved in an insulated gate semiconductor device such as an insulated gate transistor. A preferred embodiment of the present invention can be fabricated from silicon material. The body of the device can comprise a partially processed wafer which in the illustrated example of an insulated gate transistor includes a first layer of one type conductivity silicon material. A second layer of opposite type conductivity silicon material is disposed atop the first layer. Either the first or the second layer can be the substrate with the other layer device being established thereon by epitaxial growth. Alternatively, the first or second layer can be used as the substrate with the other layer being established by doping the substrate with the appropriate type dopant impurity by, for instance, diffusion or implantation doping techniques. A first region of the one type conductivity is disposed within the second layer and forms a PN junction therewith. A second region of opposite type conductivity is disposed wholly within the first region and forms a first PN junction therewith. An insulated gate structure is disposed over a portion of the first region and in response to an appropriate applied bias potential, a channel is established through the first region for facilitating the flow of opposite type conductivity carriers from the second region to the second layer. A first surface of the device comprises a portion of the second layer and a portion of the first and second regions. A cathode electrode is disposed on the first surface in ohmic contact with the first and second regions. An anode electrode is disposed in ohmic contact with the first layer.

A heavily doped grid of the one type conductivity semiconductor material is disposed within the second layer beneath the first surface proximate the first PN junction between the first and second regions. The grid can comprise a plurality of discrete one type conductivity regions at least one of which overlaps and is directly connected to said first layer and another of which overlaps and is directly connected to the first region. It is preferred that the discrete grid regions be electrically interconnected to form a substantially equipotential grid network. It is also preferred that each grid region be heavily doped and equidistantly spaced from and beneath the surface of the device such that the grid comprises an equipotential plane which is substantially parallel to the upper surface of the device. The grid can be separately connected to an external electrode, or alternatively, can be coupled via the first region to the cathode electrode.

The grid provides an alternate current path for the flow of one type conductivity carriers between the anode and cathode electrodes. The grid reduces the portion of one type conductivity carriers flowing into